REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 23, 25, 28, and 35-51 are in this application. Claims 1-22, 24, 26-27, and 29-34 have been cancelled. Claims 23, 25, and 28 have been amended to more broadly recite the present invention. Claims 38-51 have been added to alternately and more broadly claim the present invention.

The Examiner rejected claims 23 and 25 under 35 U.S.C. §103(a) as being obvious over Akram et al. (U.S. Patent No. 6,022,750) in view of Kishimoto (U.S. Patent Publication No. US 2001/0048980 A1). For the reasons set forth below, applicant respectfully traverses these rejections.

Claim 23 recites:

> "a die having:
> "a semiconductor structure . . .; and
> "an interconnect structure connected to the semiconductor structure . . . ; and
> "a test structure including:
> "a first conductive region having a first surface connected to an exterior surface of the interconnect structure and an opposing second surface;
> "an insulation region having a first surface and an opposing second surface, the first surface of the insulation region contacting the second surface of the first conductive region; and
> "a second conductive region having a first surface and an opposing second surface, the first surface of the second conductive region contacting the second surface of the insulation region, the second conductive region being electrically isolated from the first conductive region."

FIG. 1 of Akram shows an exploded view of a temporary package 10 that is used to test a die 12. As shown in FIGS. 2 and 3 of Akram, when die 12 is placed in temporary package 10, a number of contact members 60 on a test interconnect 16 are brought into contact with the pads of die 12 so that the electrical operation of die 12 can be tested and verified.

As further taught by Akram, a test interconnect can suffer from defects that occur during fabrication, and from repeated use (the same test interconnect is used over and over to test a large number of dice). These defects can have an affect on the electrical characteristics of the test interconnect which, in turn, can skew the test results for a die. Thus, in order for a test interconnect to provide valid test data, the values of the electrical parameters of the test interconnect must fall within relatively narrow ranges. (See from column 1, line 65 to column 2, line 23 of Akram.)

As a result, Akram teaches that a large number of test structures can be formed on test interconnect 16, not to test the operation of die 12, but to verify the operation of test interconnect 16. As further taught by Akram, one of the test structures that can be formed on test interconnect 16 is a capacitive test structure that measures the capacitance of insulating layer 66 shown in FIG. 4 of Akram. (See column 7, lines 43-44 of Akram.)

As shown in FIG. 12 of Akram, one approach to measuring the capacitance of insulating layer 66 is to form a capacitor test structure 82 which has a lower plate 120 formed on test interconnect 16, a dielectric layer 122, and an upper plate 118. Thus, to measure the capacitance of insulating layer 66, dielectric layer 122 is formed to have the same thickness and from the same material as insulating layer 66. Further, to operate capacitor test structure 82, dedicated electrical paths are formed between the upper and lower plates 118 and 120 and external leads 38 on test package 10.

In rejecting the claims, the Examiner pointed to die 12 shown in FIGS. 1-4 of Akram as constituting the die required by claim 23, and test interconnect 16 shown in FIGS. 1-4 of Akram as constituting the test structure required by claim 23. The Examiner noted that Akram does not show the details of die 12, but pointed to the Kishimoto reference as teaching the conventional structure of a die, including a semiconductor structure and an interconnect structure.

In further rejecting the claims, the Examiner pointed to lower plate 120 of capacitive test structure 82 shown in FIG. 12 of Akram as constituting the first conductive region required by claim 23. In addition, the Examiner pointed to

dielectric layer 122 shown in FIG. 12 of Akram as constituting the insulation region required by claim 23, and upper plate 118 shown in FIG. 12 of Akram as constituting the second conductive region required by claim 23.

The elements of Akram's capacitive test structure 82, however, can not be read to be the first conductive region, the insulation region, and the second conductive region required by claim 23. As noted above, claim 23 requires that the first conductive region be connected to an exterior surface of the interconnect structure of the die.

However, as shown in FIG. 3 of Akram, capacitive test structure 82 is not formed on an exterior surface of the interconnect structure of die 12, but instead is formed on a surface of test interconnect 16 some distance away from the interconnect structure of die 12. Thus, since lower plate 120 is not connected to an exterior surface of the interconnect structure of die 12, claim 23 is patentable over Akram in view of Kishimoto. In addition, since claims 25 and 51 depend directly from claim 23, claims 25 and 51 are patentable over Akram in view of Kishimoto for the same reasons as claim 23.

New claim 38 recites:

> "a die having:
> "a semiconductor structure that includes a substrate and a plurality of devices that are formed in and on the substrate; and
> "an interconnect structure connected to the semiconductor structure to electrically interconnect the devices to realize a circuit, the interconnect structure having a top surface, a number of bond pads, a dielectric structure that contacts the bond pads, a first metal region that contacts the dielectric structure, and a second metal region that contacts the dielectric structure; and
> "a region of silicon having a bottom surface connected to only a non-conductive region of the top surface of the interconnect structure, and being spaced apart from the bond pads."

New claim 38 is believed to be patentable for the same reasons that prior claim 2 was allowable. In addition, since claims 39-50 depend either directly or

indirectly from claim 38, claims 39-50 are patentable for the same reasons as claim 38.

Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are requested.

Respectfully submitted,

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